Observational demonstration of a low-cost fast Fourier transform spectrometer with a delay-line-based ramp-compare ADC implemented on FPGA

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Abstract

In this study, a novel type of Fourier transform radio spectrometer (termed as all-digital radio spectrometer; ADRS) has been developed in which all functionalities comprising a radio spectrometer including a sampler and Fourier computing unit were implemented as a soft-core on a field-programmable gate array (FPGA). A delay-line-based ramp-compare analog-to-digital converter (ADC), which was completely digital, was used, and two primary elements of the ADC, an analog-to-time converter (ATC) and a time-to-digital converter (TDC), were implemented on the FPGA. The sampling rate of the ADRS f and the quantization bit rate n are limited by the relation $\tau = 1/(2^n f)$, where τ is the latency of the delay element of the delay-line. Given that the typical latency of the delay element implemented on FPGAs is $\sim$10 ps, the adoption of a low-quantization bit rate, which satisfies the requirements for radio astronomy, facilitates the realization of a high sampling rate up to $\sim$100 GSa s^{-1}. In addition, as the proposed ADRS does not require a discrete ADC and can be implemented on mass-produced evaluation boards, its fabrication cost is much lower than that of conventional spectrometers. The ADRS prototype was fabricated with values of $f = 600$ MSa s^{-1} and $n = 6.6$ using a PYNQ-Z1 evaluation board, with a τ of 16.7 ps. The performance of the prototype, including its linearity and stability, was measured, and a test observation was conducted using the Osaka Prefecture University 1.85$-$m mm–submm telescope; this confirmed the potential application of the prototype in authentic radio observations. With a cost performance 10 times better ($\sim$800 USD GHz^{-1}) than conventional radio spectrometers, the prototype facilitates cost-effective coverage of intermediate frequency bandwidths of $\sim$100 GHz in modern receiver systems.

Key words: instrumentation: spectrographs—telescopes

1 Introduction

Heterodyne observation in radio astronomy is a powerful technique for investigating interstellar medium (ISM) using frequency-related information detected from molecular emission lines. Typically the technique provides a high spectral resolution of $F/\Delta F > 10^6$, where F is a central frequency and ΔF is the frequency resolution of the system; therefore the technique is often used for detailed analysis of the dynamic states of ISM by resolving their Doppler velocity in $\sim 0.1\,\mathrm{km\,s^{-1}}$ (e.g., Nishimura et al. 2018; Fujita et al. 2021; Tokuda et al. 2020). However, since the frequency coverage is typically limited to $BW/F \sim 0.05$, where BW is the bandwidth observed by the system in parallel, the technique is inefficient for wider bandwidth observations, including multi-line observations and unbiased surveys for detection of redshift. Recently, wide-bandwidth heterodyne receivers for detection of radio frequency (RF) and intermediate frequency (IF) have been developed with an output bandwidth of $\sim 20\,\mathrm{GHz}$ (Kojima et al. 2018, 2020; Masui et al. 2020; Yamasaki et al. 2020). Moreover, to extend the survey coverage of molecular line mappings toward expansively distributed giant molecular clouds, multibeam receivers have been created using wide-bandwidth technologies (Minamidani et al. 2016; Nishimura et al. 2020a). These multibeam receivers can now attain total IF output bandwidths of $\sim 100\,\mathrm{GHz}$; however, this expansion requires development of associated back-end systems with wider bandwidths and lower costs.

Improvements in the bandwidths of digital radio spectrometers have been possible because of the development of enhanced computing techniques. Typically, radio spectrometers comprise two parts: (i) a sampler that digitizes the voltage of the input radio signal and (ii) a calculator that computes the power spectrum from the sampled data. Consequently, achieving a wider spectrometer bandwidth requires faster samplers and more powerful calculators. The AC240 fabricated by Acquiris was the first digital spectrometer with a bandwidth of 1 GHz to be commercially developed for applications in radio astronomy (Benz et al. 2005). During the following decade, several spectrometers with bandwidths of several GHz were developed (Klein et al. 2006, 2012; Kamazaki et al. 2012; Stachnik et al. 2013; Jiang et al. 2014, 2016, 2020; Hickish et al. 2016; Iwai et al. 2017), all of which possessed a discrete analog-to-digital converter (ADC) for the sampler and a field programmable gate array (FPGA) for the calculator. Even with a narrow back-end bandwidth, the total bandwidth of the back-end system can be increased using multiple back-ends connected by an adequate IF circuit. Thus, the cost of the spectrometer is an essential consideration in realizing a
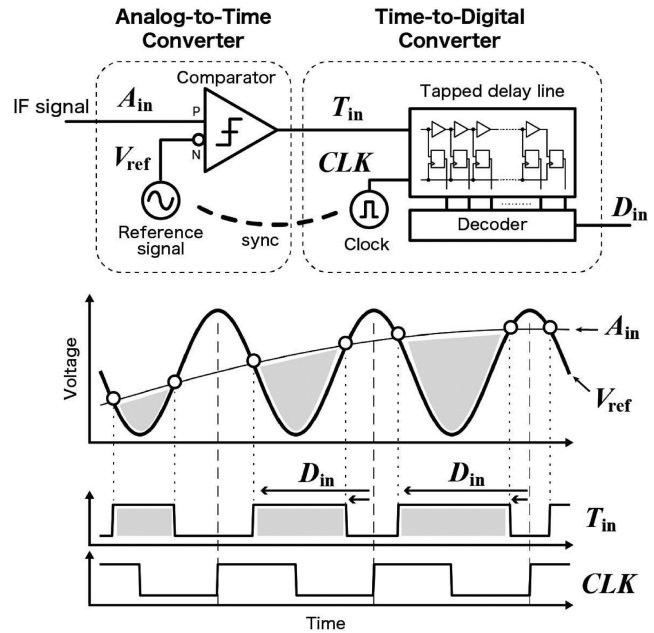

Fig. 1. Upper: Architecture of the delay-line-based ramp-compare type ADC comprising an ATC and a TDC. Lower: Timing diagram of the ADC. A_{in} indicates the analog voltage input to the ATC, and V_{ref} indicates the reference signal used for the voltage comparison in the ATC. T_{in} shows the output signal of the ATC that is input to the TDC, and CLK is the clock signal used in the TDC. D_{in} is calculated by detecting the positive and negative edges of the T_{in} signal at the decoder. The phases of V_{ref} and CLK are synchronized during the operation.

wideband back-end system. To reduce the cost of spectrometers, graphics processing unit (GPU) spectrometers that use GPUs instead of FPGAs for the calculation of fast Fourier transforms (FFTs) are proposed (e.g., Mizuno et al. 2014; Chennamangalam et al. 2014; Minamidani 2019).

This paper addresses this need for cost reduction by implementing all the functionalities of radio spectrometers within a single FPGA chip (hereafter, an all-digital radio spectrometer; ADRS). To implement an ADC function on an FPGA as a soft-core, this study adopts a delay-line-based ramp-compare fully digital ADC (L. A. Kamas & J. Rivoir 2004;[1] Li et al. 2009). The ADC mainly comprises two parts—an analog-to-time converter (ATC) and a time-to-digital converter (TDC)—and all of the components constituting the ATC and TDC can be implemented on FPGAs (Wu et al. 2007; Erni et al. 2013; Pałka et al. 2014; Homulle et al. 2015, 2016; Xiang et al. 2018). Figure 1 presents the principle of operation of the ramp-compare ADC with a delay-line. The ATC is implemented using the continually repeating reference signal (e.g., sine wave) and the comparator, which compares the voltages of the reference and the input IF signals. The delay-line type TDC (D. R. Hoppe 1984;[2] Tancock et al. 2019) is

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[1] L. A. Kamas & J. Rivoir 2004, US Patent 671540B1.

[2] D. R. Hoppe 1984, US Patent 4439046.
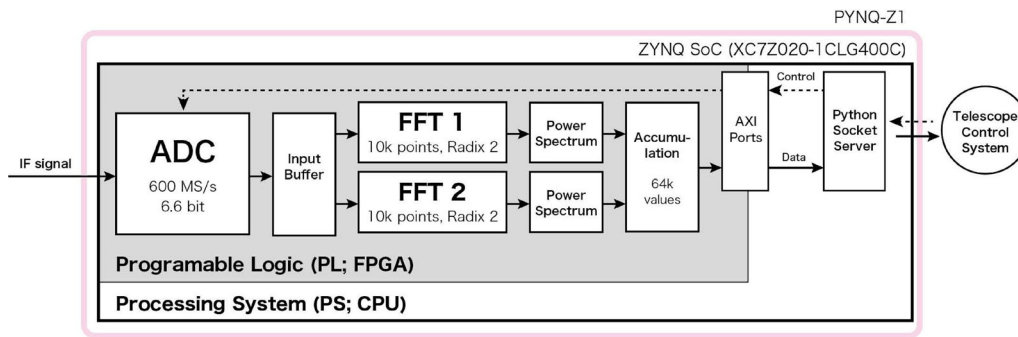
Fig. 2. Architecture of the prototype of the ADRS with a sampling frequency of 600 MSa s^{-1}. The solid arrows indicate the flow of data for the processed IF signal, and the dashed arrows indicate the flow of the ADC control. (Color online)

used for the ADC. Although ADCs with a sampling rate of over 1 GHz (Homulle et al. 2016), multiple input channels (Xiang et al. 2018), and working under an ultra-low temperature (Homulle et al. 2016; Xiang et al. 2018) have been realized on FPGAs to-date, the implementation of radio spectrometers using the ADC has not been reported. In this paper, a radio spectrometer equipped with a delay-line-based ramp-compare type ADC has been developed to examine the feasibility for authentic radio observations. The sampling rate was 600 MSa s^{-1} with a quantization bit rate of 6.6. The ADC and an FFT core were implemented on an FPGA (XC7Z020-1CLG400C, Xilinx) mounted on an evaluation board (PYNQ-Z1, Digilent). Section 2 presents the architecture of the developed spectrometer including the operating principle of the ramp-compare ADC, its implementation within the FPGA, and the design of the FFT calculation. Subsection 2.1 provides the details of the principle of operation. Section 3 provides descriptions of the calibration of the spectrometer, and section 4 presents the results of the performance evaluation and the test observations. Section 5 contains the summary of the paper.

2 System architectures

A Digilent PYNQ-Z1 board was used for the ADRS demonstrations. This board was selected for the prototype because of its low cost, easy handling by the Linux operating system, and its provision of a well-prepared PYNQ software framework. The PYNQ-Z1 board contains an FPGA chip (ZYNQ XC7Z020-1CLG400C, Xilinx), which is a programmable system-on-a-chip (SoC) containing both an FPGA and a central processing unit (CPU) that can run Linux. PYNQ is a Python-based open-source framework that provides access to the FPGA controlling and communicating with the logics implemented on the FPGA. Figure 2 illustrates the overall architectures of the 600 MSa s^{-1} ADRS implemented on the PYNQ-Z1 board. In the ADRS, both ADC and FFT are implemented within the FPGA. The accumulated power spectra are downloaded to the Python
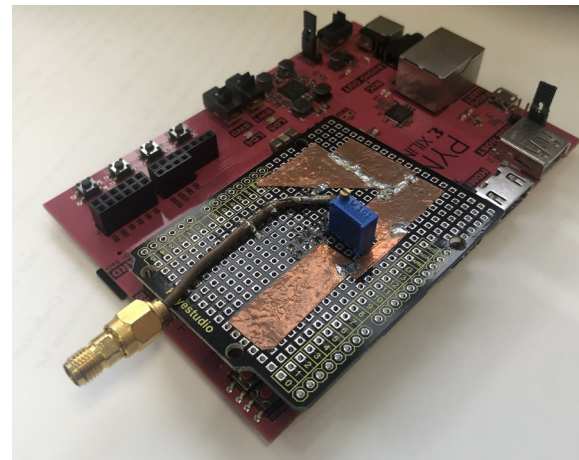
Fig. 3. Photograph of the prototype of the ADRS. (Color online)

server via an advanced extensible interface (AXI) port connection, and the network delivers the data to the telescope control system. Figure 3 presents a photograph of the ADRS prototype. The dimensions of the prototype are 88 mm × 124 mm, and its typical power consumption under ADC and FFT operation is ∼4 W. Its specific architectures are described in the following subsections.

2.1 Delay-line-based ramp-compare analog-to-digital converter core

Figure 1 presents the operating principle of the delay-line-based ramp-compare type ADC used in this study. The basic concept of the converter is the same as that used by Homulle, Regazzoni, and Charbon (2015). There are two main components in the ADC: the ATC and the TDC. The ATC contains a comparator and a reference signal generator. The low-voltage differential signaling (LVDS) element is used for the comparator by disabling its termination resistor. The analog input signal, A_{in}, is connected to the positive port of the LVDS. The output of the mixed-mode clock manager (MMCM) primitive is used for the reference signal, V_{ref}. Because the MMCM output is a square wave,

it is first output via general-purpose input-output (GPIO) connector of the PYNQ-Z1 board before passing it through an RC filter implemented on the interface board to generate the triangular wave; thereafter, the signal is directed to the negative port of the LVDS element. The comparator outputs the signal, T_{in}, of the high-level (or low-level) voltage when the voltage of the positive port is higher (or lower) than that of the negative port. The TDC comprises a delay-line and a decoder. The delay-line monitors two pulses, T_{in} and a clock signal, CLK, and detects the time offset between the negative and positive edges of the T_{in} pulse and the positive edge of the CLK pulse. The phase calibration described in subsection 3.1 synchronizes the phases of the V_{ref} and CLK during operation. Assuming that the time resolution of the TDC is τ, the sampling frequency, f, and the quantization bit rate, n, are restricted by the following relation [see also equation (1) in Li et al. (2009)]:

$$\tau = \frac{1}{2^n f}. \tag{1}$$

The delay-line is implemented using the carry connections as delay elements and flip-flops (FFs) to maintain the condition of the T_{in} signal. The delay time, τ, of each carry element for the XC7Z020-1CLG400C is 16.67 ps, and a maximum of 200 chains can be implemented within the same clock domain in the FPGA. Thus, in theory, an ADC with $(f, n) = (600\,\mathrm{MSa\,s^{-1}}, 6.6\,\mathrm{bit})$ and $(60\,\mathrm{GSa\,s^{-1}}, 1\,\mathrm{bit})$ can be realized on the FPGA chip. This paper reports a prototype with a sampling rate of $f = 600\,\mathrm{MSa\,s^{-1}}$, whereas another prototype with $f = 60\,\mathrm{GSa\,s^{-1}}$ will be reported in a separate paper (T. Matsumoto et al. in preparation). A delay-line with 200 elements was implemented. In the decoder, the output signal from the delay-line (0–199 bit) is first separated into the anterior (0–99 bits) and posterior (100–199 bit) halves containing the positive and negative edges of the T_{in}, respectively, and then the numbers of high-level bits in each 100-bit signal of the TDC code are counted using look-up tables (LUTs). The decoder converts the detected TDC code into a digitized input voltage, D_{in}, according to the calibration table, which is measured before operation (see subsection 3.2). A 300-MHz clock drives both the ATC and the TDC. The TDC outputs the positive and negative edges of the T_{in} signal as two sampling values, which provides an ADC sampling rate of 600 MSa s^{-1}.

2.2 FFT core

This study used a Radix-2 algorithm with the decimation-in-time (DIT) method to program and implement a real-time 1024 point FFT core. Two FFT cores operating with a 300 MHz clock were used to calculate the ADC code

of 600 MSa s^{-1}. Because the DSP48E1 digital signal processing slice can calculate the multiplication of the integers of 25 and 18 bit within one clock, 25 bits were assigned for the input and temporary values during the FFT calculations with 18 bits assigned for the twiddle factor. The values were processed as fixed-point numbers, and the twiddle factors for each FFT calculation were stored in the block random access memories (BRAMs). A series of FFT calculations provided a power spectrum of 512 frequency points. Thereafter, the power spectra were accumulated 65536 times corresponding to an integration time of 111.8 ms (see also figure 2). Finally, the integrated power spectrum was stored in the BRAM, which was accessible from the CPU via the AXI connections. Since the prototype demonstrates a utilization rate of FPGA elements that is below 36%, the PYNQ-Z1 boards can be used to implement a spectrometer with spectral channels exceeding 1024 points.

2.3 Data acquisition server

The Python-based socket server program has been developed to provide the power spectra to the telescope control system. The integrated power spectrum stored in the BRAM was downloaded to the CPU via AXI ports, using the Python library pynq.[3] The ADC calibrations and data download from the ADRS were controlled via the server program from socket clients such as telescope control systems.

3 System calibrations

The ADC requires two calibrations, corresponding to time and voltage domains, before its operation. Homulle, Visser, and Charbon (2016) summarized the basic concept of the calibration procedures. The following subsections describe the calibration procedures and the results for the ADRS prototype.

3.1 Phase calibration

The ramp-compare ADC requires the phases of the reference signal in the ATC and the clock in the TDC to be synchronized. The ADC implemented in this study used the reference signal, V_{ref}, which is generated by the MMCM in the FPGA and is shaped as a triangular wave through the RC filter implemented in the external circuit, before being returned to the LVDS input of the FPGA. On the other hand, the clock signal, CLK, is generated by the same MMCM and is internally connected to the TDC. Hence, significant differences exist between the paths of the V_{ref} and CLK, and the

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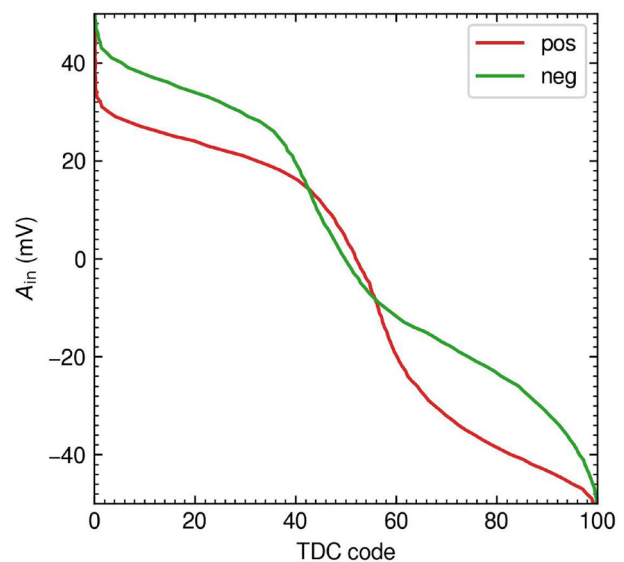[3] ⟨https://pynq.readthedocs.io/⟩.
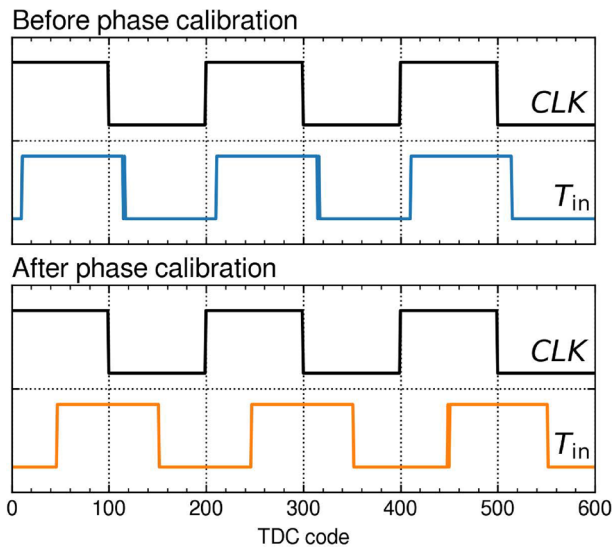
Fig. 4. Timing chart of the T_{in} signal output from the TDC. The upper and lower figures show the examples before and after the calibration. (Color online)


Fig. 5. Graph of the conversion relation from the TDC code, T_{in}, to the input bias voltage, A_{in}. The calibration curves for the positive and negative edges of the T_{in} signals are indicated in red and green, respectively. (Color online)

phase of the V_{ref} must be aligned via the calibration process. This study implemented the programmable delay element, IDELAYE2, within the wire of the T_{in} signal between the ATC and TDC. The signal input to the IDELAYE2 primitive is output by a delay of 0–1600 ps, and during operation this delay can be programmed in 32 levels. Figure 4 contains the timing chart of the T_{in} signal before and after calibration. Here, an input bias, A_{in}, of 0 V is used. The T_{in} signal is aligned after calibration, and the positive and negative edges are seen to be located at the center of the anterior and posterior halves corresponding to TDC counts of 50 and 150, respectively.

3.2 Amplitude calibration

The reference signal, V_{ref}, is not an ideal triangular wave; thus, its actual shape must be measured and corrected appropriately. The shape of the V_{ref} is measured by applying a constant voltage to A_{in} and measuring the TDC code, T_{in}. The results of the calibration measurements are provided in figure 5 and indicate the conversion relation from the TDC code, T_{in}, to the input bias, A_{in}. It is expected that the conversion curve of the ideal and most efficient triangular wave will be a straight line; however, the line produced by the ADRS prototype is wavy. The error from the ideal straight line is greater in the ADRS prototype proposed in this paper than in that reported by Homulle, Visser, and Charbon (2016), although both architectures are almost identical. This is regarded to be because the transmission lines used for the reference signal of the ADRS prototype were originally designed for digital communications and were not
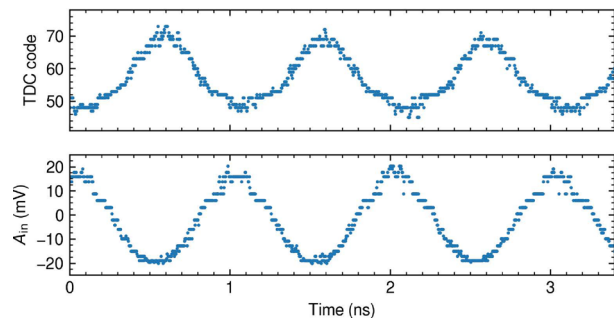
Fig. 6. TDC code and input voltage (A_{in}) digitized by the ADRS prototype for a sinusoidal period of 1 MHz. (Color online)

intended for high-frequency analog signal handling purposes. This could be enhanced by re-designing the outer circuit considering the actual GPIO line parameters, such as parasitic resistance and parasitic conductance. Broadly, the gap from the straight line causes the nonlinearity of the ADC, as normal ADCs assume an output ADC code of equally spaced interval values. To avoid this nonlinearity, this paper adopted fixed-point numbers for the ADC output code, D_{in}. The measured T_{in} value was decoded to the D_{in} of the signed fixed-point value with a bit number of 25; this length is identical to that used in the FFT calculations. The measured conversion table was stored in the BRAM, and the decoding was operated in one clock. Although the output of the ADC code is not an equally spaced interval value when using this configuration, in principle it produces an ADC code that is free of systematic errors, including gain error, offset error, and integral nonlinearity (INL).
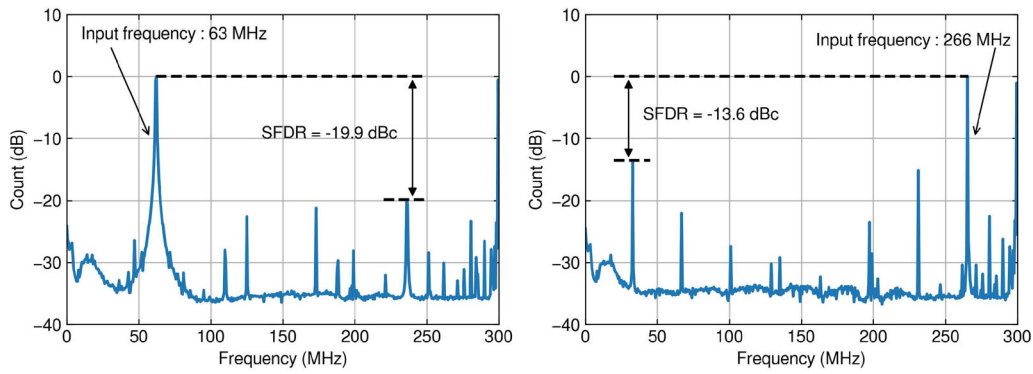
Fig. 7. Measured SFDR of the ADRS prototype for sinusoids of 63 MHz (left) and 266 MHz (right). (Color online)

Figure 6 shows the measured TDC code, T_{in}, and the ADC code, D_{in}.

Fluctuations in the operating temperature of the FPGA are considered to cause changes in the calibration parameters described above. The resulting effects on the accuracy of the power and frequency of the obtained spectrum necessitate further investigation.

4 Evaluation of performance

4.1 General performance

Homulle, Regazzoni, and Charbon (2015) and Homulle, Visser, and Charbon (2016) investigated the performance of a delay-line-based ramp-compare ADC implemented on an FPGA. This subsection describes the results of the performance evaluations of the ADRS prototype particularly in the context of its application in radio astronomy observations.

Figure 7 illustrates the plots of the power spectra measured by the ADRS prototype. The signals of continuous sine waves generated by the signal generator at frequencies of 63 and 266 MHz were input to the ADRS. Spurious-free dynamic ranges (SFDRs) of -19.9 and -13.6 dBc were measured for input frequencies of 63 and 266 MHz, respectively, while the same frequencies generated signal-to-noise-and-distortion ratios (SNDRs) of -10.0 and -5.4 dB, respectively. The effective number of bits (ENOB) was calculated to be 1.4 and 0.6 for input frequencies of 66 and 266 MHz, respectively, using the following equation:

$$ENOB = \frac{SNDR - 1.76}{6.02}. \qquad (2)$$

In general, the ENOB of the delay-line-based ramp-compare ADC is low, especially for the higher-frequency side. Homulle, Visser, and Charbon (2016) reported that the typical ENOB of their 1.2-GSa s^{-1} 6.6-bit ADC at an input frequency of 100 MHz is $\sim$3. An ENOB is lower if the noise floor level is higher or the level of spurious signal
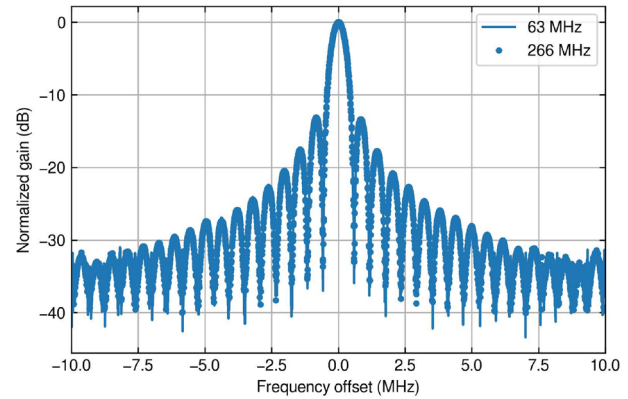

Fig. 8. Frequency response of the ADRS prototype for frequencies of 63 and 266 MHz. The rectangular window function is used. (Color online)

is higher. For the ADRS prototype, the input analog signal is sampled with an unequally spaced time and is quantized with an unequally spaced voltage, and these two factors cause the increase of the quantization error in the output ADC code. The level of spurious signal is increased if the quantization error is correlated to the time, while in the other case the noise floor level is increased. In this paper, the level of the noise floor and the spurious level of the ADRS prototype are both higher than in the model used by Homulle, Visser, and Charbon (2016); consequently, the ENOB of the ADRS prototype is lower than that reported by Homulle et al. (2016). This is mainly due to the non-ideality of the reference signal (see figure 5). However, the low ENOB of the ADRS seems not to affect the linearity dynamic range of input power critically (see below). Furthermore, the system noise temperature and the antenna temperature of the celestial object are correctly measured by the ADRS prototype (see subsection 4.2), suggesting that the low ENOB does not affect the accuracy of the radio observations.

Figure 8 shows the measured frequency response of the ADRS prototype. The full width at half maximum (FWHM) of the main lobe was measured to be 515.8 kHz, which
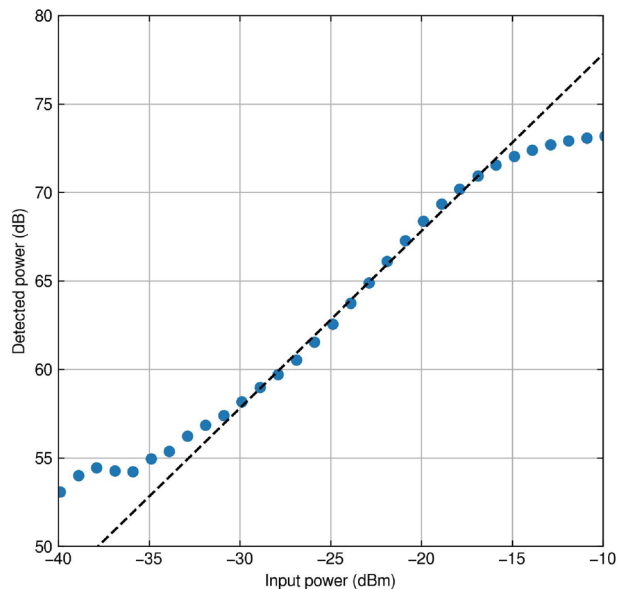
Fig. 9. Relationship of the input power and the detected power levels of the ADRS prototype. The dashed line indicates the ideal linear response for reference. (Color online)
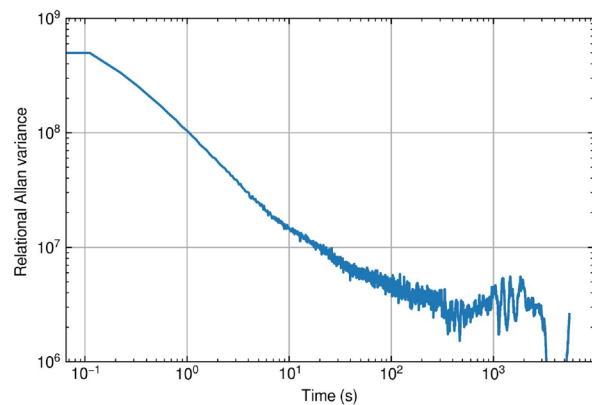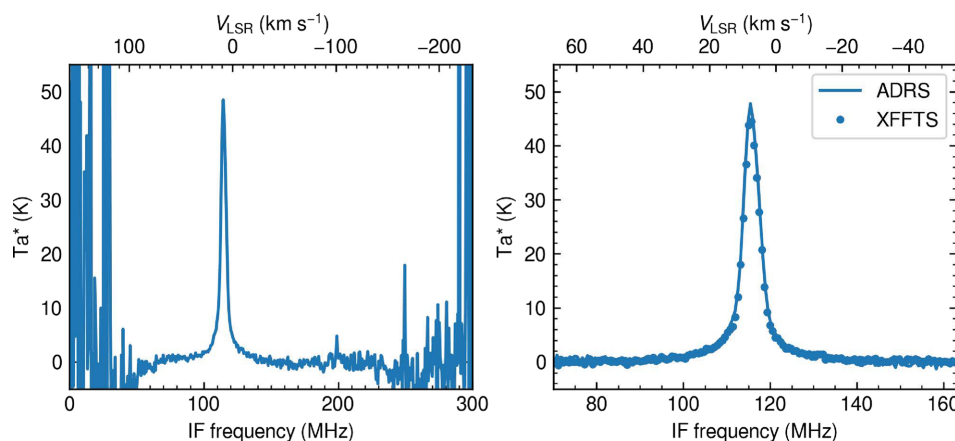

Fig. 10. Relational Allan variance plot of the ADRS prototype. Data with a frequency separation of 15 MHz was used. (Color online)

4.2 Test observations

First-light observations were conducted in 2020 December using the Osaka Prefecture University 1.85m mm–submm telescope (Onishi et al. 2013; Nishimura et al. 2020b) with a 230-GHz band receiver (Masui et al. 2020; Yamasaki et al. 2020) installed at the Nobeyama Radio Observatory. The receiver had an output bandwidth of 2 GHz, and a low-pass filter (LPF), Mini-Circuits VLF-180 with a bandwidth of 180 MHz, was inserted prior to the ADRS prototype. The frequency interval of the spectrum obtained by the ADRS prototype was 585.9 kHz, corresponding to the velocity resolution of $0.76 \, \mathrm{km \, s^{-1}}$ for the 230-GHz band. The IF output from the receiver was simultaneously recorded by RPG XFFTS (Klein et al. 2012), and the observation results were compared. The system noise temperature including atmosphere, T_{sys}, was measured by the ADRS prototype to be $\sim 600 \, \mathrm{K}$, which represents a difference of $< 10\%$ to the XFFTS value. The weather conditions during the investigation were cloudy. Figure 11 shows the spectrum of the $^{12}\mathrm{C}^{16}\mathrm{O}$ $J = 2$–1 line towards Ori-KL obtained by position-switching observations with an integration time of 180 s. After subtracting the baseline, the peak temperature of the spectrum was the same as the XFFTS result within an error of 10%, and the shape of the spectrum is consistent with the XFFTS result. However, the observation efficiency, ε, of the ADRS prototype is 20% lower than that of the XFFTS, where ε is defined by the following equation:

$$\varepsilon = \frac{T_{\mathrm{sys}}}{T_{\mathrm{rms}}\sqrt{dt df}}, \qquad (3)$$

where T_{rms} is the rms of the spectrum, dt is the integration time, and df is the frequency resolution. The lower efficiency of the ADRS prototype is considered to be mainly attributed to environmental noise emanating from the telescope instruments. Because of fabrication deficiencies in the

corresponds to a bin width of 0.88, and the level of the side lobe was measured to be −13.1 dB. No window functions were implemented for the ADRS prototype. These performances are consistent with the frequency response for the rectangular window, whereas the implementation of window functions or digital pre-filters such as a polyphase filter bank is an area for future study. The response curves were almost identical over the entire 300-MHz bandwidth of the ADRS prototype, and it was confirmed that the frequency response of the spectrometer demonstrated no negative effects when the delay-line-based ramp-compare ADC was adopted.

Figure 9 presents the results of linearity evaluation for the detected power of the ADRS, which were obtained by measuring the spectra of a laboratory noise source under various power inputs. The detected power demonstrated a linear response for an input power range from −30 to −17 dBm with an error below 10%. This dynamic range of 13 dB is wide enough for heterodyne observations that require a dynamic range of typically ∼5 dB, according to the power ratio of a source and calibrator operating at room temperature.

The spectroscopic Allan variance was evaluated by measuring and processing the spectrum of the noise source, resulting in an Allan time of >100 s (figure 10). A frequency separation of 15 MHz was used for the analysis. During the measurements, the room temperature fluctuated by ∼1 K, which is similar to the observation condition at the location of the 1.85-m radio telescope.

Fig. 11. Observed spectrum of $^{12}C^{16}O$ $J = 2$–1 toward Ori-KL. Left: Entire spectrum obtained by the ADRS prototype. Right: Zoomed-in view of the $^{12}C^{16}O$ $J = 2$–1 line. The line and dots indicate the spectrum obtained by the ADRS and XFFTS, respectively. (Color online)

shield of the prototype ADRS, its ground-level position was affected by environmental noise from the servomotors and cryocooler of the receiver. From this observation, the basic concept of the ADRS was confirmed to be feasible for application in the field of radio astronomy; however, improvements in noise immunity are necessary to enable efficient observations comparable with those obtained from commercial spectrometers.

5 Summary

This study developed an ADRS, which is a novel radio spectrometer based on a single FPGA chip that implements a delay-line-based ramp-compare ADC and FFT as soft-core. The operating principle of the ADC and the implementations of the ADC and FFT soft-core on the PYNQ-Z1 evaluation board were presented in detail. The first ADRS prototype-based radio spectrometer was developed with a sampling rate of 600 MHz and a quantization bit rate of 6.6. Following investigations into its performance, the stability of the ADRS for application in astronomical observations has been confirmed. Experimental validation was performed by observing the $^{12}C^{16}O$ $J = 2$–1 line toward a star-forming molecular cloud using the 1.85-m radio telescope with a 230-GHz band receiver. The obtained spectrum produced a shape that was consistent with that obtained by the XFFTS simultaneously within an error of $< 10\%$. Because of the low cost of the PYNQ-Z1, the cost performance of the prototype is around 800 USD GHz^{-1}, which is more than 10 times lower than that of other radio spectrometers. Thus, the economic and performance feasibility of implementing the ADRS to cover all IF output from modern receiver systems such as FOREST, which is achieving a bandwidth of $\sim$100 GHz, has been confirmed.

In principle, increasing the sampling rate, f, of the delay-line-based ramp-compare ADC by reducing the quantization bit rate, n, allows the extreme solution of $(f, n) = (60 \text{ GSa s}^{-1}, 1 \text{ bit})$ to be implemented using a PYNQ-Z1 board. Furthermore, using shorter delay elements to implement the TDC could result in an ADRS with an even higher sampling rated. The XC7Z020-1CLG400C FPGA used in this paper was created in a 28-nm process, whereas some of the more modern FPGAs involve 16-nm processes. It is considered that the delay time of the carry chain element is roughly proportional to the process size; therefore, using an FPGA resulting from a smaller process could produce an ADRS with a very high sampling rate of $>100 \text{ GSa s}^{-1}$.

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